

What is claimed is:

1. An electrode structure of a carrier substrate of a semiconductor device for solder-bonding the semiconductor device to a main substrate, wherein a recess is provided in a central area of the electrode, and said electrode further having, on a circumferential wall surface surrounding said recess of said central area, a through portion passing through bet surrounding said recess of said central area in said wall surface.
2. The electrode structure of the carrier substrate of the semiconductor device according to claim 1, wherein said electrode is hemispheric configuration having a flange portion and having a concentric hemispheric hollow portion thereinside, wherein said hemispheric portion of said electrode being fitted into a hemispheric recess provided on an outer surface of said carrier substrate of said semiconductor device, and said electrode being fixedly attached to said carrier substrate so that said flange portion abuts said outer surface of said carrier substrate.
3. The electrode structure of the carrier substrate of the semiconductor device according to claim 2, wherein said through portion passing through between said recess and said outer portion of said wall surface being at least one slit portion provided in said flange portion and said wall surface of said electrode adjacent to said flange portion.
4. The electrode structure of said carrier substrate of said semiconductor device according to claim 1, wherein said

electrode is cylindrical having a flange portion and having a concentric cylindrical hollow portion said reinside, said cylindrical portion of said electrode being fitted into a cylindrical recess provided on an outer surface of said carrier substrate of said semiconductor device, and said electrode is fixedly attached to said carrier substrate so that said flange portion abuts said outer surface of said carrier substrate.

5. Said electrode structure of said carrier substrate of said semiconductor device according to claim 4, wherein said through portion passing through between said recess and said outer portion of said wall surface being at least one slit provided in said flange portion and said cylindrical wall surface of said electrode adjacent to said flange portion to a position close to a bottom.

6. The electrode structure of the carrier substrate of the semiconductor device according to claim 1, wherein a package of said semiconductor device is of a BGA (ball grid array) type.

7. The electrode structure of the carrier substrate of the semiconductor device according to claim 1, wherein a package of said semiconductor device is of a CSP (chip scale package) type.

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